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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,141	03/29/2004	Craig Barrack	250338-1510 (S-3009)	2157

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EXAMINER
VU, THONG H

ART UNIT	PAPER NUMBER
2619	

MAIL DATE	DELIVERY MODE
03/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,141	BARRACK ET AL.	
	Examiner	Art Unit	
	Thong H. Vu	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-7 Canceled. Claims 8-20 are pedning.

Claim Rejections - 35 USC § 103

Claims 8-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sah et al [Sah 7,047,374 B2] in view of Ross [2004/0199729 A1].

2. Claim 8, Sah discloses A method of accessing Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM) memory storage employed in a packet switch, the DDR SDRAM memory having a plurality of memory banks for storing packet data of a plurality of packets [Sah, DDR SDRAM, col 5 lines 8-18], the method comprising steps of:

a. segmenting packet data into variable size burst units [Sah, various sizes, col 7 line 15];

b. sequencing a plurality of burst unit memory write operations (i.e.: I/O operation) ensuring that each burst unit memory write operation writes packet data to a memory bank different from the previous burst unit memory write operation [Sah, sequence or contiguous address request, for different I/O modes, col 12 lines 9-35; the previously activated page, col 13 lines 45-56];

c. sequencing a plurality of burst unit memory read operations (i.e.: I/O operation) ensuring that each bust unit memory read operation reads packet data from a memory bank different from the previous burst unit memory read operation [Sah, sequence or contiguous address request, for different I/O modes, col 12 lines 9-35; the previously activated page, col 13 lines 45-56];

Sah also taught the window protocol [Sah, col 7 line 26]. However Sah does not explicitly detail

d. arranging the plurality of sequenced burst unit memory write operations in a plurality of write windows;

e. arranging the plurality of sequenced bust unit memory read operations in a plurality of read windows; and

f. performing memory access operations interleaving the write windows with the read windows.

In the same endeavor, Ross taught an arbitrator handling the dynamic reordering of memory requests using DDR SDRAM [Ross, 0004]; a read/write interleave concurrent access to a window [Ross 0105-0106]

Therefore it would have been obvious to an ordinary skill in the art at the time the invention was made to incorporate the read/write interleave concurrent access to a window as taught by Ross into the Sah's apparatus in order to utilize the DDR SDRAM operation process.

Doing so would provide an effective address re-mapping ensures that the vector is distributed across the memory sub-system in a way that meets the requirements of the interleaving.

3. Claim 9, Sah-Ross disclose segmenting packet data in respect of packets received via a plurality of input switch ports prior to storing the packet data into the memory storage [Sah, port switches, col 4 lines 60-67].

4. Claim 10 Sah-Ross disclose a prior step of: enforcing packet acceptance control [Sah, enforce cache consistency, col 9 line 7].

5. Claim 11 Sah-Ross disclose selectively accepting a packet, and selectively discarding another packet [Sah, filter, col 7 lines 37-57].

6. Claim 12 Sah-Ross disclose preferentially scheduling write burst units corresponding to a packet from one of a packet received via a high bandwidth input port, a high quality-of-service packet, a packet of a particular type of service, an alarm packet, and a signaling packet [Sah, scheduler, col 19 line 55].

7. Claim 13 Sah-Ross disclose delaying scheduling of write burst units totaling less than ten memory access cycles long to a single bank [Sah, scheduler, col 19 line 55]. Claim 14 Sah-Ross disclose segmenting packet data in respect of packets stored in the memory storage for transmission via a plurality of output switch ports [Sah, port switches, col 4 lines 60-67].

8. Claim 15 Sah-Ross disclose preferentially scheduling read burst units corresponding to packets from one of: a packet to be transmitted via a high bandwidth output port, a high quality-of-service packet, a packet of a particular type of service, an alarm packet, and a signaling packet as inherent feature of scheduling.

9. Claim 16 Sah-Ross disclose delaying scheduling of read burst units corresponding to packets destined to a congested output port [Sah, scheduler, col 19 line 55].

10. Claim 17 Sah-Ross disclose delaying scheduling of read burst units totaling less than ten memory access cycles long to a single bank [Sah, scheduler, col 19 line 55].

11. Claim 18 Sah-Ross disclose segmenting packet data into at least four as inherent feature of segmenting.

12. Claim 19 Sah-Ross disclose segmenting packet data into burst units transferring at least 49 bytes of packet data as inherent feature of segmenting.

13. Claim 20 Sah-Ross disclose employing windows at least 128 memory access cycles long as inherent feature of window protocol.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong H. Vu whose telephone number is 571-272-3904. The examiner can normally be reached on 6:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thong H Vu/
Primary Examiner, Art Unit 2619